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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,624	06/15/2001	Ian Wylie	WYLIE 5	8470
27964	7590	11/06/2003	EXAMINER	
HITT GAINES P.C. P.O. BOX 832570 RICHARDSON, TX 75083			KIELIN, ERIK J	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/882,624

Applicant(s)

WYLIE, IAN

Examiner

Erik Kielin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) none is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This action responds to the Amendment filed 12 March 2003 (Paper no. 13).

#### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-32 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for an interface separating the first and second portions of the source/drain regions only if the materials are different, i.e. polysilicon and single crystal silicon, does not reasonably provide enablement for an interface separating the first and second portions of the source/drain regions for all materials. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims.

While it is acknowledged that Applicant argues in the Amendment filed 12 March 2003 (Paper no. 13),

“Second, as the material of the first and second portions of the source/drain regions was formed in separate steps, and not a single step as shown in the references, an interface must exist.”

This is factually in error. For example, epitaxial silicon is frequently grown on stock single crystal silicon substrates. **No interface exists** because the deposited silicon becomes an extension of the single crystal substrate, even though plural steps are used to make the silicon:

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Czochralski growth and cutting and polishing to form the bulk silicon wafer, and epitaxial growth to grow additional silicon on the wafer. Another example is atomic layer epitaxy or deposition (ALE or ALD). In ALE, monolayers are deposited upon monolayers in cycles until the desired thickness is achieved; yet no interface exists between layers. For at least these factual reasons, Applicant's observation that "an interface must exist" merely by use of plural steps to form the source/drain regions is erroneous.

Finally while Examiner acknowledges that a "line" is shown between the first and second portions of the source/drain regions in the Figs. 1, 11, and 12, such a line exists specifically because the materials are different, i.e. polysilicon and monocrystalline silicon. Were the polysilicon crystallized or grown epitaxially using the Si substrate as the template, no such interface would exist. For this reason, the claims are only enabled in scope to the use of separate materials, i.e. polysilicon and single crystal silicon, there being no mention of an interface in the specification or the part it may play in the instantly claimed device. (See instant specification paragraphs [0024] and [0042] through [0044].) Moreover, in the absence of a description of "the interface," electrical contact might not be made between the portions.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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5. Claim 1 recites the limitation “the first and second portions” in line 6. There is insufficient antecedent basis for this limitation in the claim. A similar problem exists with each of the independent claims, 7, 12, 17, 21, and 27.

6. Each of the independent claims 1, 7, 12, 17, 21, and 27 also uses the terminology “first portion” and “second portion” to describe both the isolation region and the source/drain regions. Accordingly, for clarity, the claims must clearly indicate whether the portion being addressed belongs to the isolation region or the source/drain regions.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-5, 7-10, **12-14**, 16, **17-19**, and **21-25** are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,043,778 (**Teng et al.**).

**Teng** discloses a semiconductor device comprising,

a semiconductor substrate **10** having N- and P-wells **14**, **16** (Fig. 7);

a gate **24** above each well in the semiconductor substrate;

a channel region **33** (Fig. 5A; col. 9, line 4);

a trench (**32** and that portion holding the part of the isolation region **20**) adjacent the channel region **33** (Fig. 3; col. 8, lines 53-58);

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an isolation region **20** formed adjacent the semiconductor substrate and located within the trench and comprising an oxide (col. 7, line 21), wherein the isolation region includes a first portion and a second post portion (shown as the narrower portion at the top of **20**, but not labeled), wherein no structural interface exists between the first and the second portions, and wherein the second portion is located over the first portion, and wherein the trench does not extend under the channel region **33**, and wherein the isolation is between the transistors indicated by the gates **24**; and

a first portion of a source/drain region **44** formed in the semiconductor substrate, and a second portion of the source/drain region **36** formed on the isolation region from polysilicon (col. 8, lines 57-58) and in contact with the second post portion but not in the semiconductor substrate, and wherein there exists an "interface" between the first and second portions of the source/drain region.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 6, 11, 15, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Teng** in view of US Patent Application 2002/0142552 A1 (**Wu**).

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The prior art of **Teng**, as explained above, discloses each of the claimed features except for forming the isolation region to extend through a transistor tub ("well").

**Wu** teaches each of the features of the independent claims except for the second portion contacting the post portion **114a** of the isolation. Note that the isolation region extends through the tubs/wells.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use form the isolation of **Teng** to extend through a tub/well, as taught by **Wu** in order to form a more thorough isolation between devices as shown in **Wu**.

11. Claims **27-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Teng** in view of Applicant's admitted prior art (**APA**).

**Teng**, as explained above, discloses all of the features of the instant invention except for specifically showing the interconnect and other active and passive devices.

Applicant indicates that Fig. 12 shows a conventional integrated circuit (paragraph [0022]) with interconnect **1220** and other active and passive devices and that one of ordinary skill is familiar with these additional elements (paragraph [0044]).

It would have been obvious to one of ordinary skill at the time of the invention to modify **Teng** to include known interconnect and active and passive device in order to form a functioning circuit, such as a DRAM, because it highly desired in the art to form whole integrated circuits rather than just parts which would, in isolation, be useless.

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12. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Teng** in view of **APA**, as applied to claim 27 above, and further in view of US Patent Application 2002/0142552 A1 (**Wu**).

The prior art of **Teng**, as explained above, discloses each of the claimed features except for forming the isolation region to extend through a transistor tub ("well").

**Wu** teaches the features as noted above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use form the isolation of **Teng** to extend through a tub/well, as taught by **Wu** in order to form a more thorough isolation between devices as shown in **Wu**.

### ***Response to Arguments***

13. Applicant's arguments filed 12 March 2003 have been fully considered but they are not persuasive.

Applicant's arguments regarding the rejection of the claims under 35 USC 112(1) are not fully persuasive. These arguments are addressed above in the rejection of the claims as not enabling in the breadth of scope presently claimed.

Applicant arguments regarding **Teng** are noted. The arguments are based upon the alleged existence of an interface in the first and second portions of the isolation region. First, this is merely a conclusory observation, and factually in error for the reasons indicated above. Second, no interface is shown in the **Teng** reference indicating that no such interface exists. Third, Applicant argues that the "line" shown between the first and second portions of the source/drain regions of instant Figs. 1, 11, and 12, qualifies as support for the limitation of the



interface between the portions of the source/drain regions. It is hypocritical for Applicant to deny the Teng reference the same right they bestow upon themselves by virtue of that shown in the drawings. In other words, the showing in Teng Fig. 7 of the **absence of an interface** in any portion of the isolation region **20** provides just as much support for the **absence of an interface**, as the showing of the line in the instant Figs. being alleged support for one. Moreover, those of ordinary skill in the materials art know well that forming an amorphous silicon oxide in contact with amorphous silicon oxide would not form an interface, as properly shown in Teng. Amorphous materials have no long-range structure and, as such, there would not necessarily exist a demarcation (interface) between portions formed in different steps. And fourth, the post portion is not formed in a separate step. Should any interface exist, it would not be between the first portion and the second post portion.

Finally in this regard, Examiner is happy to consider evidence --not argument-- showing that the Teng structure has an interface between the first portion and the second post portion of the isolation region.

### ***Conclusion***

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Erik Kielin  
Primary Examiner  
November 5, 2003